REMARKS

This is a full and timely response to the outstanding nonfinal Office Action mailed on June 16, 2008. Reconsideration and allowance of the application and presently pending claims 1, 3-22 and 24 are respectfully requested.

In the Office Action, claims 1 and 3-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. More particularly, the previously added feature "charging current of the first output capacitor is the difference between the pulse current output from the front-end converter and the pulse current drawn by the first buck converter and the second buck converter" is not found in the original disclosure. Claims 1 and 3-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Bourdillon (U.S. Pat. No.6,552,917, "Bourdillon" hereinafter), in view of Hailey (U.S. Pat. No.6,664,657, "Hailey" hereinafter) in further view of Huang et. al. (U.S. Pat. No. 6,344,979, "Huang" hereinafter).

In response thereto, claims 1, 15, 18 and 22 have been amended. It is believed that no new matter is added by way of amendments made to claims. For at least the foregoing reason, Applicants respectfully submit that claims 1 and 3-22 and 24 patently define over prior art of record and reconsideration of this application is respectfully requested.

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Examiner Interview

Applicants first wish to express his sincere appreciation for the time that Examiner Wallis spent with Applicants' Attorney during a telephone discussion on **Oct. 30, 2008** regarding the outstanding Office Action. Applicants believe that certain important issues were identified during the telephone discussion, and that they are resolved herein. During that conversation, the Examiner indicated that it would be potentially beneficial for Applicants to make the amendments herein. Thus, Applicants respectfully request that Examiner carefully considers this response and the amendments.

Discussion of Claim Rejection Under 35 U.S.C. 112

Claims 1 and 3-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

In response thereto, Applicants have deleted the previously added feature "charging current of the first output capacitor is the difference between the pulse current output from the front-end converter and the pulse current drawn by the first buck converter and the second buck converter" from the claims 1, 15 and 18, which render the rejection moot.

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Discussion of rejection to claims under 35 U.S.C. §103(a)

Claims 1 and 3-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Bourdillon, in view of Hailey in further view of Huang.

In response thereto, applicants respectfully traverse the rejection based on the following arguments.

In order to avoid misunderstanding, the feature "charging current of the first output capacitor..." is deleted from the present application and the feature "so as to reduce the ripple current on the first output capacitor" is added in the application.

Independent claims 1, 15, 18 and 22 are recited as followed:

Claim 1 recites in part "A power supply with multiple outputs, comprising:

...

a time delay synchronous control circuit, *for controlling a delay time between the time the front-end converter begins to have a pulse current to the first output capacitor and the time the first buck converter and the second buck converter being turned on is adjusted so as to reduce the ripple current on the first output capacitor*, ..."

Claim 15 recites in part "A power supply with multiple outputs, comprising:

...

a time delay synchronous control circuit, for controlling the first buck converter and the second buck converter alternatively drawing one of the two pulse currents from the first output capacitor during the time when every two pulse of the output current of the

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front-end converter are provided, and during the time of each pulse of the output current of the front-end converter, only one of the first buck converter and the second buck converter drawing the pulse current from the first output capacitor, *so as to reduce the ripple current on the first output capacitor, and the front-end converter is an LLC-SRC.*"

Claim 18 recites in part "A time delay synchronous control method for a power supply with multiple outputs,...

adjusting a delay time between the time the front-end converter begins to have the pulse output current to the output capacitor and the time the first buck switch and the second buck switch being turned on *so as to reduce the ripple current on the first output capacitor*."

Claim 22 recites in part "A power supply with multiple outputs, comprising:

...a time delay synchronous control circuit, for controlling a time the converter begins to have a pulse current to the output capacitor and a time the buck converter being turned on so as to reduce the ripple current on the output capacitor"

In response thereto, applicants believe that the following arguments have been presented and have not been considered in previous office action, but have been discussed and agreed during the interview with the undersigned and the Examiner.

As stated in lines 5-9 in paragraph [0004] in specification, the present application intends to resolve a problem occurred in AAPA (i.e. Fig.1); in other words, the present application

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minimizes ripple current of an output capacitor of a front-end DC/DC converter shown in AAPA. However, in Fig.3, in Bourdillon, generally, if two of three switches S1-S3 are turned on concurrently, for example, S1 and S2, output current of secondary side of transformer T1 is not equal to the sum of currents passing through circuits 311 and 313, but equal to the current passing one of circuits 311 and 313, which has a lower output voltage. Since there are switches S1, D1, S2, D2, S3, D3 disposed between the secondary side and the output loads, the output current of the secondary side of the transformer only passes through the circuit having lowest output voltage among the circuits 311, 313 and 315. Accordingly, only circuit 313 has a current passing through if it has lowest output voltage, when S1 and S2 are turned on. Thus, to minimize ripple current of the secondary side of the transformer, Bourdillon needs to select the circuit having maximum output voltage among the circuits 311, 313 and 315 as the converter's output. Furthermore, in Bourdillon, non-concurrently turning on of switches S1, S2 and S3 doesn't benefit reducing the ripple current of the output capacitor of the front-end DC/DC converter, which is intended to be resolved by the present application. Though, from lines 2-7, in col.5, in Bourdillon, in general, there may be some overlap between the ON and OFF times of the sequential controlled switches just in order to achieve soft-switching and prevent the converter from being unloaded. Hence, as discussed in aforementioned underlined portion, since Bourdillon is incapable of resolving the problem, which the present application intends to resolve, any artisan is not motivated to combine Bourdillon and AAPA.

Additionally, even if Bourdillon and AAPA could be combined, this proposal combination still fails to teach, suggest or disclose the time delay synchronous control circuit as claimed in claims 1, 15, 18 and 22. In other words, independent claims 1, 15, 18 and 22 are not rendered

obvious by the combination of Bourdillon and AAPA because a prima facie case of obviousness is not well established, and thus patentable.

In the Office Action, Heiley reference is cited to remedy the deficiency of the combination of the AAPA and Bourdillon. Applicants point out that the disclosure of the Heiley upon which the Examiner relied for the deficiency is **the common characteristics of the capacitor**. However, as defined in the claims 1, 15, 18 and 22, the time delay synchronous control circuit controls a delay time between the time the front-end converter begins to have a pulse current to the first output capacitor and the time the first buck converter and the second buck converter being turned on is adjusted so as to reduce the ripple current on the first output capacitor, neither AAPA, Bourdillon, Heiley alone nor the combination thereof, have disclosed the aforesaid features.

In response thereto, applicant respectfully traverses the rejection based on the aforesaid arguments.

Since claims 3-14, 16-17, 19-21 and 24 are dependent claims, they should be patentable for the reason that they contain all limitations of their patentable base independent claims 1, 15, 18 and 22.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1 and 3-22, and 24 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

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Jiawei Huang
Registration No. 43,330

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949)-660-0809

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